ABSTRACT

[0036] A resistive cross point memory cell array comprising a plurality of word lines, a plurality of bit lines, a plurality of cross points formed by the word lines and the bit lines, and a plurality of memory cells, each of the memory cells being located at a different one of the cross points, wherein a first bit line comprises a distributed series diode along an entire length of the bit line such that each of the associated memory cells located along the first bit line is coupled between the distributed series diode and an associated word line.